UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,018	08/07/2001	James W. Blatchford JR.	5-1-1-23-1	3037

7590 08/25/2003

Docket Administrator
Agere Systems Inc.
P.O. Box 614
Berkeley Heights, NJ 07922-0614

EXAMINER	
RUGGLES, JOHN S	

ART UNIT	PAPER NUMBER
1756	2

DATE MAILED: 08/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,018	BLATCHFORD ET AL.	
	Examin r	Art Unit	
	John Ruggles	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *1-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A (1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Objections

Claims 1-19 are objected to because of the following informalities: while lines 2 and 4-5 of claim 1 recite "energy sensitive material" (repeated in claims 4, 17, and 19), lines 1-2 of claims 2-3 refer to this same material as "energy sensitive resist material" (repeated in claims 8 and 15). In order to be consistent, the same language should be used throughout the claims, because both phrases refer to the same material. Claims 2-19 are dependent on claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 lacks antecedent basis for "the first pattern", found in line 4. It is unclear whether this phrase is intended to refer to the image of a pattern introduced into the energy sensitive material as a latent image recited in line 2 or a different pattern formed by subsequent developing of the image of a pattern to form a visible image in the energy sensitive material, as suggested in line 4. For the purpose of this Office action and in order to advance prosecution of this application, this phrase has been interpreted to mean --a developed first pattern--. However, claim 1 must still be amended in response to this rejection. Furthermore, "introducing" of the image recited in line 2 is interpreted in light of the disclosure to mean --exposing-- (e.g., as described at lines 16-19 on page 1, etc.) and "transferring" of the pattern found in line 9 is interpreted in light of the disclosure to mean --etching-- (e.g., using conventional expedients as described at lines 29-30 on page 3, etc., which includes anisotropic etching found at line 17 on page 1). Claims 2-19 are dependent on claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 9-13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao, et al. (US Patent 5,747,196) in view of Mixon, et al. (US Patent 5,688,634).

Chao teaches fabrication of a phase shift mask (PSM) for lithography by successively forming a light transmissive thin film 34 and a light blocking thin film 37 on a transparent substrate 31. Forming a patterned resist layer 36 on the light blocking thin film 37, as shown in Figure 5A. Forming of the patterned resist is understood to include patterned exposure of an energy sensitive resist material and subsequent developing of the exposed resist material to form a first pattern having features of a first size. The patterned resist 36 is used as an etching mask to anisotropically etch the uncovered portions of the light blocking thin film 37 and the light transmissive thin film 34, leaving remaining parts 35 and 33, respectively, as shown in Figure 5B. The first size of the pattern resist 36 is then reduced by isotropic etching of both the upper and side surfaces thereof, leaving a remaining patterned resist 38, which have features of a second size as shown in Figure 5C. Figure 5D shows the result of a subsequent anisotropic etching step to transfer the pattern of the remaining resist 38 having features of a second size into the underlying light blocking thin film 35 (column 4, line 41 to column 5, line 5). A conventional method of forming the initial resist pattern involving direct writing exposure of a computer controlled electron beam onto a electron beam positive resist followed by developing to remove the exposed portions of the resist is shown in Figure 1A and disclosed at column 1, lines 38-50.

While contemplating the sequence of steps recited by instant claims 1, 3, 9-10, and 12-13, including isotropic etching to reduce the size of the developed resist, Chao does not specify using a liquid isotropic etchant for this step.

Mixon describes a lithographic process relating to fabrication of a device (e.g., on a Si semiconductor substrate, etc., which is considered to be a semiconductor device) or lithographic

mask (e.g., chrome on a glass substrate, etc., which is also considered to be an optical device) by patterned exposure and developing of an energy sensitive resist material (having a matrix polymer which is substantially soluble in the developing agent), followed by transfer of the pattern into an underlying substrate (column 1, lines 16-21 and 58-67). The resist is typically positive acting and is sensitive to radiation chosen from a variety of wavelengths (e.g., deep ultraviolet (DUV), electron beam, ion beam, x-ray, etc., column 3, lines 34-36). Contemplated processes include mask or maskless primary pattern delineation, as well as pattern replication or secondary pattern delineation (column 6, lines 38-40). Literature data suggests that the radiation dosage can be reduced during exposure by subsequent forced developing to thin the unirradiated resist (column 7, lines 16-19). While Mixon uses interruptive developing involving plural separate developing steps to limit resist film loss, it is clearly acknowledged that further treatment in the developer solution of the previously developed resist will result in erosion of the unirradiated portions and reduce the developed resist pattern size (column 7, line 58 to column 8, line 22). So, the developer is considered to function as a liquid isotropic etchant expected to be useful for reducing the size of the remaining developed resist pattern features. The resist can be baked between exposing and developing to improve sensitivity and developing characteristics, but the baking temperature should be kept below both the glass transition temperature and the decomposition temperature of the resist polymers to preserve the resist image (column 7, lines 22-46). Baking after developing helps to remove residual developing solvent from the resist and can optionally be carried out during subsequent plasma etching using the resist as an etching mask, because the plasma etching implicitly causes heating of the resist (column 8, lines 24-28).

Table 1 in column 11 shows 1.8-54.2% film loss (size reduction) for resist patterns after developing, depending on baking and developing conditions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the lithographic process taught by Chao with the subsequent size reduction of the developed resist pattern using a liquid isotropic etchant (by further developer treatment) described by Mixon. This is because (1) Chao used isotropic etching for developed resist pattern size reduction and liquid etchants or solvents, such as developing solutions, are known to cause isotropic removal or etching of resist (also called film loss) as described by Mixon and (2) both Chao and Mixon relate to the same art of lithographic manufacture of an optical lithographic mask by exposure and developing of a positive resist usable with electron beam exposure, subsequent size reduction of the developed resist pattern features using isotropic etching, then etching of an underlying substrate through the reduced size resist pattern as an etching mask. Furthermore, Mixon describes that baking of the developed resist helps to remove residual developing solvent while baking of the resist before reducing of the developed resist caused by isotropic etching (using further developer treatment) is expected to improve sensitivity and characteristics towards the developer/isotropic etchant. Mixon also described that keeping the baking temperature below the glass transition temperature of the resist polymers would be expected to preserve the resist image.

Claims 4-5, 8, 14, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao and Mixon and further in view of McKee (US Patent 5,804,088).

Neither Chao nor Mixon specifies forming of the resist on either an inorganic antireflective or a polysilicon intermediate layer formed over the substrate.

McKee shows a lithographic process for fabricating a semiconductor device that involves use of one or more intermediate layers between a substrate and an overlying resist. The process includes exposure and developing of the resist to a first minimal linewidth, isotropic etching of the developed resist pattern and/or underlying intermediate layer to reduce the linewidth to a second smaller sublithographic size, then etching of one or more underlying layers through the reduced width developed resist pattern and/or intermediate layer as an etching mask (column 1, lines 12-14 and column 2, lines 30-37). Figure 2a shows a silicon (Si) substrate 202 covered by an oxide layer 204 (oxidized silicon), a polysilicon (polycrystalline silicon) layer 206, an inorganic buried antireflective layer (BARC) of titanium nitride (TiN) 208, and an overlying resist layer 210. After exposing, developing, and baking, the resist 211-212 linewidths are shown as W and L, respectively, in Figure 2c. Isotropic etching reduces the sizes of the resist 213-214 linewidths by $2\Delta W$, as shown in Figure 2e. Anisotropic etching removes the exposed portions of the BARC layer 208 to complete the etching mask for subsequent etching of underlying polysilicon 206. Polysilicon 206 is then anisotropically etched using this reduced size etching mask (column 2, line 37 to column 3, line 47). Another embodiment carries out the narrowing isotropic etching of the BARC layer from 821-822 to 823-824 using a wet or liquid isotropic etchant, as shown in Figures 8c and 8d (column 5, lines 59-63). Many other variations are contemplated that use the intermediate layer as a BARC, an etchstop, a sacrificial layer for linewidth reduction, or as a liftoff layer for an overlying resist (column 6, lines 62-67). The resist can be stripped before etching through the narrowed BARC alone as an etching mask

(understood to function as a hardmask during etching using a selective etchant, column 7, lines 1-4). Furthermore, the etch chemistries and conditions, the exposure wavelength (in addition to I-line described in these embodiments), as well as the resist and antireflective compositions, can each be varied while using this same approach to reduce the attainable pattern linewidth to a sublithographic dimension (column 7, lines 6-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the lithographic process taught by Chao and Mixon with one or more intermediate layers of (1) polycrystalline silicon, (2) inorganic antireflection material which may also function as a hardmask layer, and/or (3) oxidized silicon as shown by McKee. This is because all of these references relate to the same art of lithographic patterning to fabricate semiconductor or optical devices by reduction of a resist pattern size to form sublithographic device features.

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao, Mixon, and McKee, and further in view of Lyons, et al. (US Patent 6,121,123).

While showing the usefulness of an inorganic antireflection coating between the substrate and the overlying resist for perfecting exposure of the resist, Chao, Mixon, and McKee do not specify that the inorganic antireflective layer should be a dielectric material comprising silicon, oxygen, and nitrogen, and do not teach forming this antireflective layer by chemical vapor deposition.

However, silicon oxynitride (SiON) is a known bottom antireflective coating (BARC) and hardmask material tuned for absorption of deep ultraviolet (DUV) light used to expose an

overlying resist and can be formed by conventional chemical vapor deposition (CVD) to create a more uniform layer than the typical spin-on BARC material as taught by Lyons (abstract and column 3, lines 30-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the SiON BARC/hardmask formed by CVD as taught by Lyons for the TiN BARC/hardmask shown by McKee, because the SiON CVD BARC/hardmask is more uniform and is tuned for DUV exposure wavelengths.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Ruggles whose telephone number is 703-305-7035. The examiner can normally be reached on Monday-Thursday and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 703-308-2464. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

John Ruggles
Examiner
Art Unit 1756

MARK F. HUFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700